

[PIPELINED LOW COMPLEXITY FFT/IFFT PROCESSOR]

Abstract of Disclosure

A pipelined, real-time N-point transform processor contains a first butterfly triplet multiplicatively connected to an output portion by way of a complex multiplier. The butterfly triplet contains a first butterfly I unit (BFI), a butterfly II unit (BFII) and a butterfly III unit (BFIII), which are connected together in series. An input port of the first BFI serves as an input port of the triplet to accept complex numbers, and an output port of the BFIII serves as an output port of the triplet. The complex multiplier accepts a complex result from the output port of the first triplet, and a coefficient provided by a control unit to generate a complex product. The output portion contains at least a second BFI, an input port of the second BFI accepting the complex product from the complex multiplier, and the output portion provides the transformed complex numbers. The control unit contains a pipeline step-count register, and the ability to provide the coefficients to the complex multiplier. The control unit controls each BFI, each BFII, each BFIII, and provides each coefficient, according to a value held in the pipeline step-count register. A reordering circuit is provided to insure that the order of the transformed complex numbers matches that of the input complex numbers.

Figures